CLAIM LISTING

This listing of claims will replace all prior versions, and listings of claims in the application:

IN THE CLAIMS

1. (Currently Amended) A buffer circuit comprising:

a plurality of memory locations to hold data;

the memory locations of the plurality of memory locations addressable across an address space;

a read pointer to point a read address of the plurality of memory locations from which to read output data;

a write pointer to point a write address of the plurality of memory locations in which to write input data;

the read and the write pointers operable responsive to respective read and write clocks to sequence the read and write addresses across the address space of the plurality of memory locations;

a control register to ~~define~~ store a nominal level as a set fill level of the buffer circuit; and

a controller to affect operation of the read pointer dependent on the write address of the write pointer, the read address of the read pointer, and the nominal level;

the controller configured to controllably activate and deactivate operation of the read pointer by electrically coupling and decoupling, respectively, a clock input of the read pointer for obtaining the read clock.

2. (Original) The circuit of claim 1, the controller operable to:

determine an amount of data in the buffer circuit based on a difference between the write address and the read address; and

enable the read pointer to increase the read address based on a difference between the amount of data determined and the nominal level.

3. (Original) The circuit of claim 2, in which the controller is further operable to at least hold the read address of the read pointer when the amount of data is determined to be less than the nominal level.

4. (Currently Amended) The circuit of claim 2 [[3]], in which the controller is further operable to decrement the read address when the amount of data is determined to be less than the nominal level.

5. (Original) The circuit of claim 3, in which the controller is further operable to advance the read address of the read pointer when the amount of data is determined to be greater than the nominal level.

6. (Original) The circuit of claim 5, in which the controller is further operable to disable the clock input to the read pointer and hold the read address upon determining the amount of data in the buffer circuit to be less than the nominal level.

Claims 7-8. (Canceled)

9. (Original) The circuit of claim 1, further comprising initialization circuitry to:

configure the write pointer with a predetermined start address for the write address; and

configure the read pointer with a beginning value based on the predetermined start address for the write address and the nominal level.

10. (Original) The circuit of claim 9, in which the beginning address for the read pointer is an address offset from the starting write address, and the offset is equal to the nominal level.

Claims 11-43. (Canceled)